Reg.No. \_\_\_\_\_\_\_\_\_\_\_\_



**UNIVERSITY**

(Karunya Institute of Technology & Sciences)

(Declared as Deemed-to-be University under Sec.3 of the UGC Act, 1956)

**Supplementary Examination – June – 2017**

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| **Code :** | **14EC2001** | **Duration :** | **3hrs** |
| **Sub. Name :** | **DIGITAL ELECTRONICS** | **Max. marks :** | **100** |

**ANSWER ALL QUESTIONS (5 x 20 = 100 Marks)**

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| Q. No. | Sub Div. | Questions | Course  Outcome | Marks |
| 1. | a. | Simplify the following equation using K-Map  F(a,b,c,d)=Σm(0,1,2,3,4,5,8,10,11) + d(14,15) | CO1 | 10 |
| b. | Simplify the following equation using Quine Mc-cluskey method  F(a,b,c,d)=Σm (4,8,10,11,12,15) + d(9,14) | CO1 | 10 |
| (OR) | | | | |
| 2. | a. | Simplify the following using Kmap  f(a,b,c,d)= Σm(0,2,4,6,8,10,11,12,13) | CO1 | 10 |
| b. | Convert (1101101101.110)2 to its decimal, octal and hexadecimal equivalent. | CO1 | 10 |
| 3. |  | Design 1x4 demultiplexer and 4x1 multiplexer and explain its function. | CO2 | 20 |
| (OR) | | | | |
| 4. | a. | Design a 2 bit magnitude comparator. | CO2 | 12 |
|  | b. | Implement and design a half adder and full subtractor circuit. | CO2 | 8 |
| 5. |  | Draw the logic circuit, characteristic table and derive the characteristic equation of SR, JK, D and T flip flop. | CO2 | 20 |
| (OR) | | | | |
| 6. | a. | Implement the following Boolean function with a multiplexer with B, C and D connected to selection lines S2 , S1, and S0  respectively.  F(A,B,C,D) = ∑ (0,1,2,3,6,7,9,11,15) | CO2 | 10 |
|  | b. | With a suitable example, explain the process of state reduction. | CO2 | 10 |
| 7. |  | Design a 3 bit ripple counter using T flip flop. | CO2 | 20 |
| (OR) | | | | |
| 8. |  | Design a 3 bit PISO shift register and draw its timing diagram. | CO2 | 20 |
|  | | **Compulsory:** |  |  |
| 9. |  | Draw the structure of PLA, PAL and PROM and briefly explain. | CO3 | 20 |

ALL THE BEST